REAL-TIME CLOCK OPTION

H316 General Purpose Digital Computer

Honeywell

Doc. No. 70130072179A
M-497

H316-12
REAL TIME CLOCK OPTION
Instruction Manual

May 1969

Honeywell

COMPUTER CONTROL DIVISION

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CONTENTS

ILLUSTRATIONS

H316-12
REAL TIME CLOCK

INTRODUCTION

This document contains a detailed description of the H316 General Purpose Computer Real Time Clock Option.

Reference Data

H316 Central Processor Description, Doc. No. 70130072176, H316 Central Processor Instruction and Diagrams, Doc. No.70130072174, and H316 Circuit Modules and Parts Manual, Doc. No. 70130072166.

Physical Characteristics

The Real Time Clock Option consists of a μ-PAC mounted in location A1BA17.

Functional Description

The Real Time Clock permits the H316 to keep track of real time by automatically incrementing the contents of memory location 00061_8. The rate is adjustable from 50 Hz to 250 Hz (every 20 ms to every 4 ms). When the contents of the tallied memory location overflow from 177777_8 to 000000_8, a standard interrupt is generated. By processing a suitable interrupt subroutine, the program can keep track of time by monitoring and counting the interrupts generated by the clock. A typical application would be keeping track of elapsed time in minutes after a particular action has been intiated by the computer. By setting the period to 16.7 milliseconds, loading $-3600_{10}(170760_8)$ into memory location 00061_8 and setting the Real Time Clock program interrupt mask, the program can keep track of one minute of elapsed time. If the subroutine reserves a memory location to be incremented every time the clock interrupt occurs, the location will accumulate a total of elapsed time in minutes.

INSTALLATION

Interconnections

All interconnections are wired directly as shown in the logic diagram provided with this manual.

THEORY OF OPERATION

General Theory

Every 20 ms to 4 ms (depending on setting), the Real Time Clock Option generates a break request. The central processor honors the request by incrementing the contents of memory location 00061_8 by one. The break request can be inhibited or enabled by OCP Instructions. When the contents of 00061_8 equal zero, the Real Time Clock activates the standard interrupt request line if the RTC interrupt mask is set.

The special complement of instructions for the Real Time Clock are described in the Honeywell 316/516 Programmers Reference Manual. These instructions are as follows:

OCP '0220	Reset program interrupt request and stop clock
OCP '0020	Reset program interrupt request and run clock
SMK '0020	Set mask
SKS '0020	Skip if RTC not interrupting

Detailed Theory

See LBD 0.147 for Real Time Clock Option logic and Figure 1 for a flow chart of the clock break and interrupt request logic. Refer to Table 1 for logic signal mnemonic designations and definitions. For description of the standard interrupt and break implementation, refer to H316 Central Processor Description. For a description of the I-Cycle (used to force an IRS or JST instruction), refer to H316 Central Processor Instructions and Diagrams Manual.

The free running multivibrator clock provides a trigger at the frequency set by the adjustable potentiometer R8. If the clear RTC flip-flop (J4, LBD 0.147) is set, each negative-going edge of the Schmitt trigger output pulses sets the RTCLK flip-flop (J2, LBD 0.147). The set output of RTCLK delivers a Real Time Clock service request (RTCLK+) to the Priority Network (B5, LBD 0.135), see H316 Central Processor Instructions and Diagrams.

RTCLK+ and TL2FF+ cause the Priority PAC Real Time Clock flip-flop to set and generate an SEXRC (Real Time Clock service request) signal and an IAD61 (interrupt address 00061_8) signal. SEXRC and $\overline{\text{IAD63}}$ (not standard interrupt address) generate PISEX and BRREQ signals (B-1 and D-1, LBD 0,134), see H316 Central Processor Instructions and Diagrams. These signals request a computer break which increments the contents of memory location 00061_8 by one.

After BRREQ has been generated and if it is determined that it was not caused by a DMC request, a CLPIL signal is generated at the end of the present instruction (EOINS) by TL4FF (M6, LBD 0.134), see H316 Central Processor Instructions and Diagrams Manual. CLPIL, in conjunction with the set condition of the Priority PAC Real Time Clock flip-flop, generates an ACKRC (acknowledge real time clock) signal (F-3, LBD 0.135), see H316 Central Processor Instructions and Diagrams.

The ACKRC signal, indicating the break request has been honored, resets the RTCLK flip-flop (LBD 0.147). In this manner, the contents of 00061_8 are incremented every period.

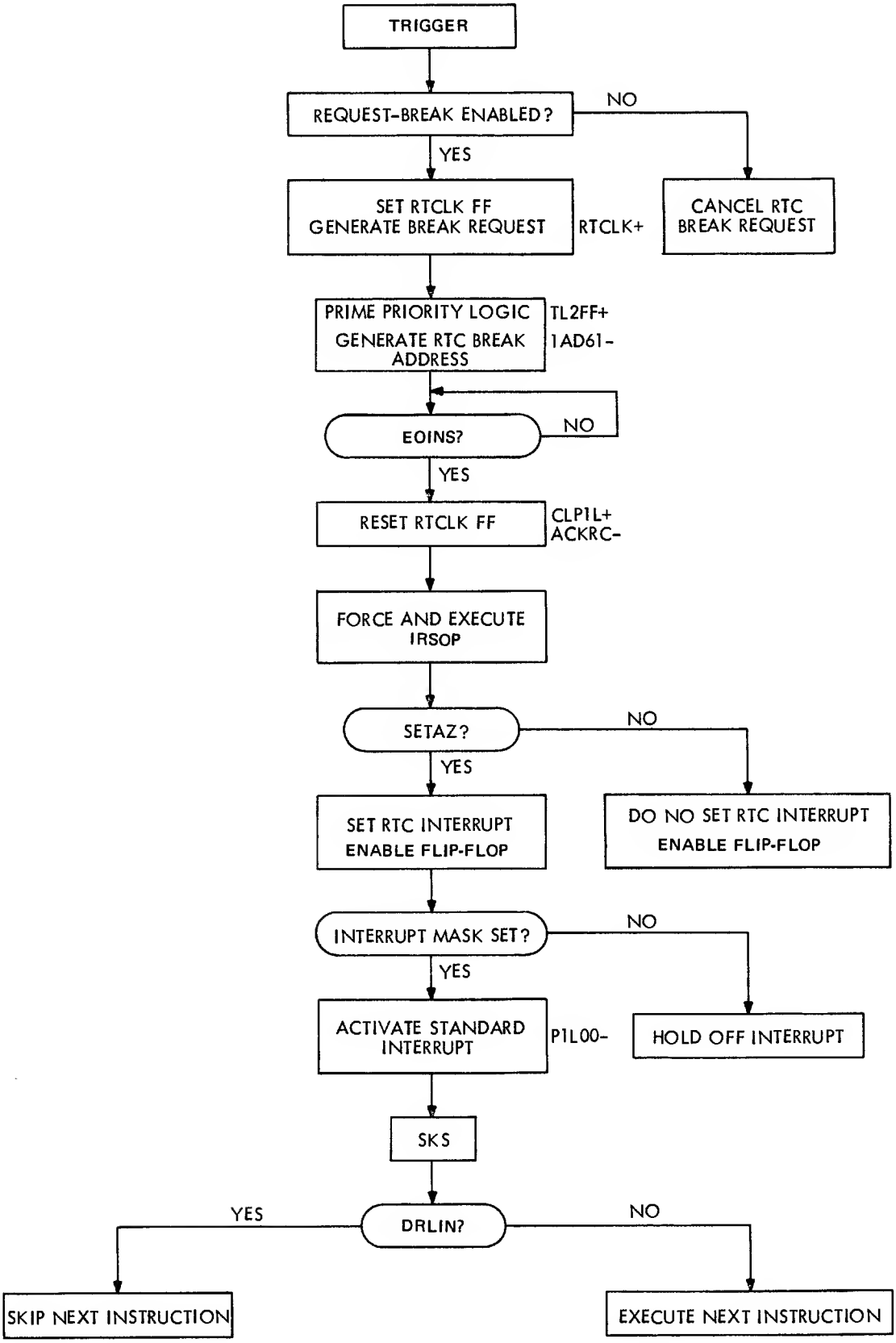
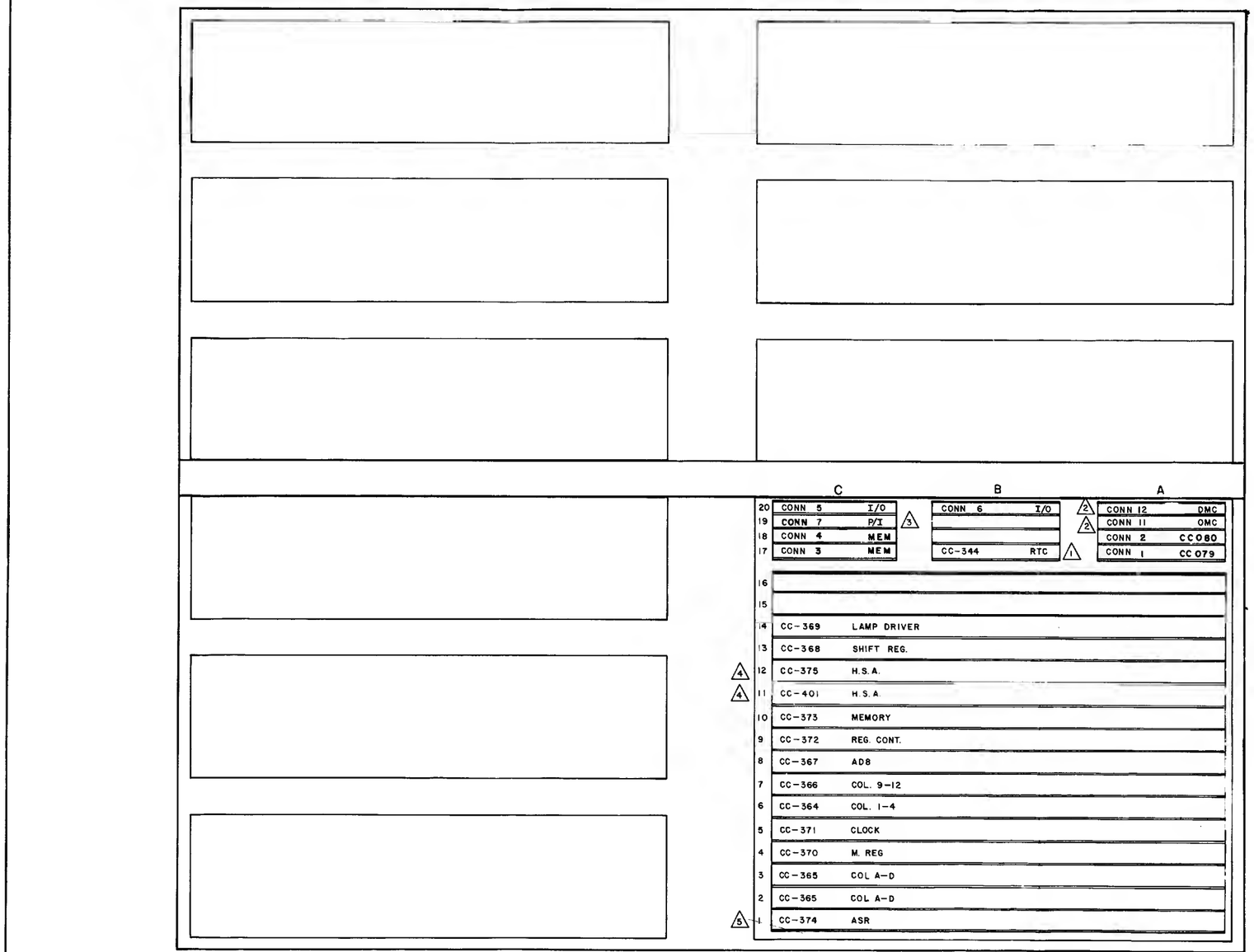


Figure 1. Real Time Clock Break and Interrupt Request Flow Chart

Table 1.
Function Index List

Mnemonic	LBD No. 0.147 Zone	Definition
OCPLS-	A3	Output control pulse. Activated by OCP Instruction
OCPRC+	F3	Signifies clock is addressed by OCP Instruction
IG063-	A5	Interrupt address is greater than 00063_8
IRSOP+	A5	IRS op code: IRS is being processed
A16FF+	H8	A-register bit 16 to control setting
ACKRC-	H2	Acknowledge Real Time Clock break request
ADB07- ADB08- ADB10- through ADB16-	A9	Address bus bits 7, 8, and 10 through 16
ADB09-	C3	Address bus bit 9. During OCP instruction: when ZERO, enable clock break request; or when ONE, disable clock break request
BREAK+	A5	BREAK flip-flop
DRLIN-	M8	Device ready signal: made ONE to signify clock is not interrupting
EOINS-	E7	End-of-instruction signal
PIL00-	M6	Standard interrupt line. Activated by clock interrupt request
RTCAD+	G9	Real Time Clock address decoder
RTCLK+	J1	Real Time Clock break request flip-flop
SETAZ+	H6	Set AZZZZ control signal. Generated by IRS Instruction
SMK01+	H8	Set mask group 1 control signal. Generated by SMK '0020 instruction
RTCEN+	F6	RTC Interrupt enable
CLRTC+	J4	Clear Real Time Clock flip-flop
RCENB+	J6	Real Time Clock Enable flip-flop, Interrupt request
RCMSK+	J8	Real Time Clock Mask flip-flop

L.B.D. NO. 0.100



NOTES:

1. 702: REAL TIME CLOCK.
2. 703: O.M.C.
3. 704: PRIORITY INT.
4. 705: H.S.A
5. 706: A9R-33

REV.	REVISIONS	CHK.
A	S.R. 54-3585	#

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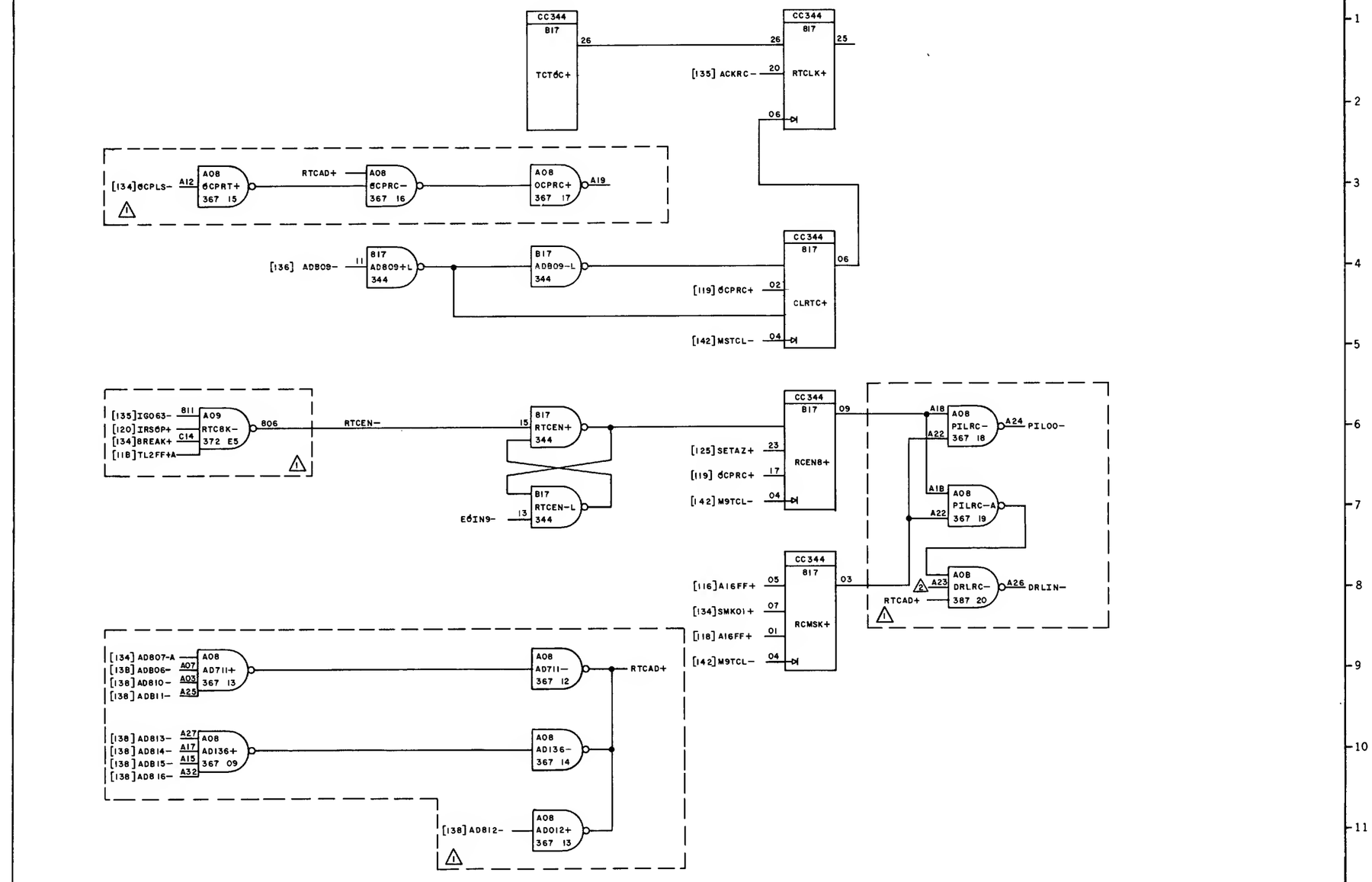
DR. D. HAMEL	DATE	
ENG. K. IZBICKI	1-20-1969	
APP.		
PROJECT NO. 55202		

TITLE
316 M.F. & M.F. OPTION
PAC LOCATION

SIZE	DWG NO.	REV.
C	70024276	A



NOTES:

1. THESE CIRCUITS ARE ALSO SHOWN ON L.B.D. 0.119
2. REMOVE GND WHEN USING RTC

REVISIONS	REV.	
	A	S.R 54-3585
CHK.		

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ENG. K. IZBICKI	2-27-69
APP.	
PROJECT NO. 55202	

TITLE
H-316-12
REAL TIME CLOCK

SIZE	DWG NO.	REV.
C	70024524	A

When the contents of 00061_8 overflow from 177777_8 to 000000_8, the RTC break generates a SETAZ signal. The trailing edge of SETAZ+ sets the Real Time Clock enable flip-flop J6 (LBD 0.147) if Interrupt enable flip-flop F6 (LBD 0.147) is set. This flip-flop is set by the following terms at gate B6 (LBD 0.147): IGO63-, IRSOP+, BREAK+, and TL2FF+. IGO63-, IRSOP+ and BREAK+ signify that an RTC break is being processed. With these conditions satisfied, the Real Time Clock Enable flip-flop is set by the trailing edge of SETAZ. Note that Interrupt enable flip-flop is reset at the end of the break by EOINS-.

If the Real Time Clock program interrupt mask flip-flop J8 (LBD 0.147) is set, the set output of the Real Time Clock interrupt request flip-flop generates PIL00 via gate L6 (LBD 0.147) to activate the standard program interrupt request line. When the computer puts out an SKS instruction addressing the Real Time Clock, the address inputs are combined (gates B9, B10, F9, F10, F11, LBD 0.147) to generate Real Time Clock address signal RTCAD. If the Real Time Clock Enable flip-flop is reset or if the mask flip-flop is reset, RTCAD causes gate L8 (LBD 0.147) to generate a DRLIN signal. If, however, the interrupt request flip-flop and the mask flip-flop are set, DRLIN is false.

The Real Time Clock Enable flip-flop J6 (LBD 0.147) must then be reset by an OCP instruction. There are two Real Time Clock OCP instructions, both of which reset the interrupt request flip-flop. OCP '0220 resets the clear RTC flip-flop J4 (LBD 0.147) to hold the RTCLK flip-flop reset. OCP '0020 sets the clear RTC flip-flop.

The OCP addresses the clock and the clock generates an RTCAD signal. RTCAD and the OCP output signal (OCPLS) generate an OCPRC signal via gate F3 (LBD 0.147). If bit 9 (ADB09) of the OCP instruction is ZERO, the trailing edge of OCPRC sets the clear RTC flip-flop. If bit 9 is a ONE, the trailing edge of OCPRC resets the clear RTC flip-flop, and the active set output of the clear RTC flip-flop holds the RTCLK flip-flop reset, thereby disabling the break request.

The Real Time Clock can be inhibited from activating the PIL00 interrupt request line by resetting the program interrupt mask flip-flop J8 (LBD 0.147). The mask flip-flop is controlled by an SMK '0020 instruction. The SMK instruction generates an SMK01 pulse which sets the mask if A16FF is set or resets the mask if A16FF is reset. The mask changes state on the trailing edge of SMK01.

The RTCLK flip-flop, the clear RTC flip-flop, the interrupt enable flip-flop, and the interrupt mask flip-flop can be reset by an MSTCL signal, which is generated by depressing the control panel MSTR CLEAR pushbutton.

PAC DESCRIPTION

A description of the Real Time Clock PAC, Model CC-344, follows.

REAL TIME CLOCK PAC, MODEL CC-344

The Real Time Clock PAC, Model CC-344 (Figure CC-344-1), contains a self-starting, free-running multivibrator clock with the associated logic circuitry.

Potentiometer R8 permits continuous variation of frequency from 50 Hz to 250 Hz. Lower frequencies are obtainable by replacing capacitor C1 with higher values.

SPECIFICATIONS

Frequency of Operation

50 Hz to 250 Hz

Frequency Stability

Over temperature range (0°C to +55°C): ±2% (max)

Input Loading

Pins 20, 11, 15, 13, 23, 17, 5, and 1:	1 unit load (each)
Pins 2 and 7:	2 unit loads (each)
Pin 4:	5 unit loads

Output Drive Capability

Pins 25 and 9:	8 unit loads (each)
Pin 3:	7 unit loads
Pin 26:	7 unit loads
Pin 6:	5 unit loads

Current Requirements

+6V: 200 mA

-6V: 30 mA

Total Power

1.4 W

Electrical Parts List

Ref. Desig.	Description	Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.27μF ±5%, 50 Vdc	70 930 316 030
C2, C3	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033μF ±20%, 50 Vdc	70 930 313 016
CR1	DIODE, SILICON	70 943 083 001
M1, M2	MICROCIRCUIT: 9097, integrated circuit	70 950 105 007
M3	MICROCIRCUIT: 946, quad NAND gate, integrated circuit	70 950 105 002
M4. M6	MICROCIRCUIT: F-04, Flip-Flop, integrated circuit	70 950 100 004
M5, M7	MICROCIRCUIT: 948, Flip-Flop, integrated circuit	70 950 105 003
R1	RESISTOR, FIXED, FILM: 1K ±2%, 1/4W	70 932 114 049
R2	RESISTOR, FIXED, FILM: 750 ohms, ±2%, 1/4W	70 932 114 045
R3	RESISTOR, FIXED, COMPOSITION: 1K ±5%, 1/4W	70 932 007 049
R4, R10	RESISTOR, FIXED, COMPOSITION: 2.7K ±5%, 1/4W	70 932 007 059
R5, R11	RESISTOR, FIXED, COMPOSITION: 1.8K ±5%, 1/4W	70 932 007 055
R6, R7	RESISTOR, FIXED, FILM: 3.9K ±2%, 1/4W	70 932 114 063
R8	RESISTOR, FIXED, FILM: 2K ±10%, 1/2W	70 933 301 008
R9	RESISTOR, FIXED, FILM: 270 ohms, ±2%, 1/4W	70 932 114 035
R12	RESISTOR, FIXED, COMPOSITION: 22K ±5%, 1/4W	70 932 007 081
Q1	TRANSISTOR S1 PNP Type (721-2)	70 943 721 002
Q2-Q5	TRANSISTOR S1 NPN Type (722-2)	70 943 722 002

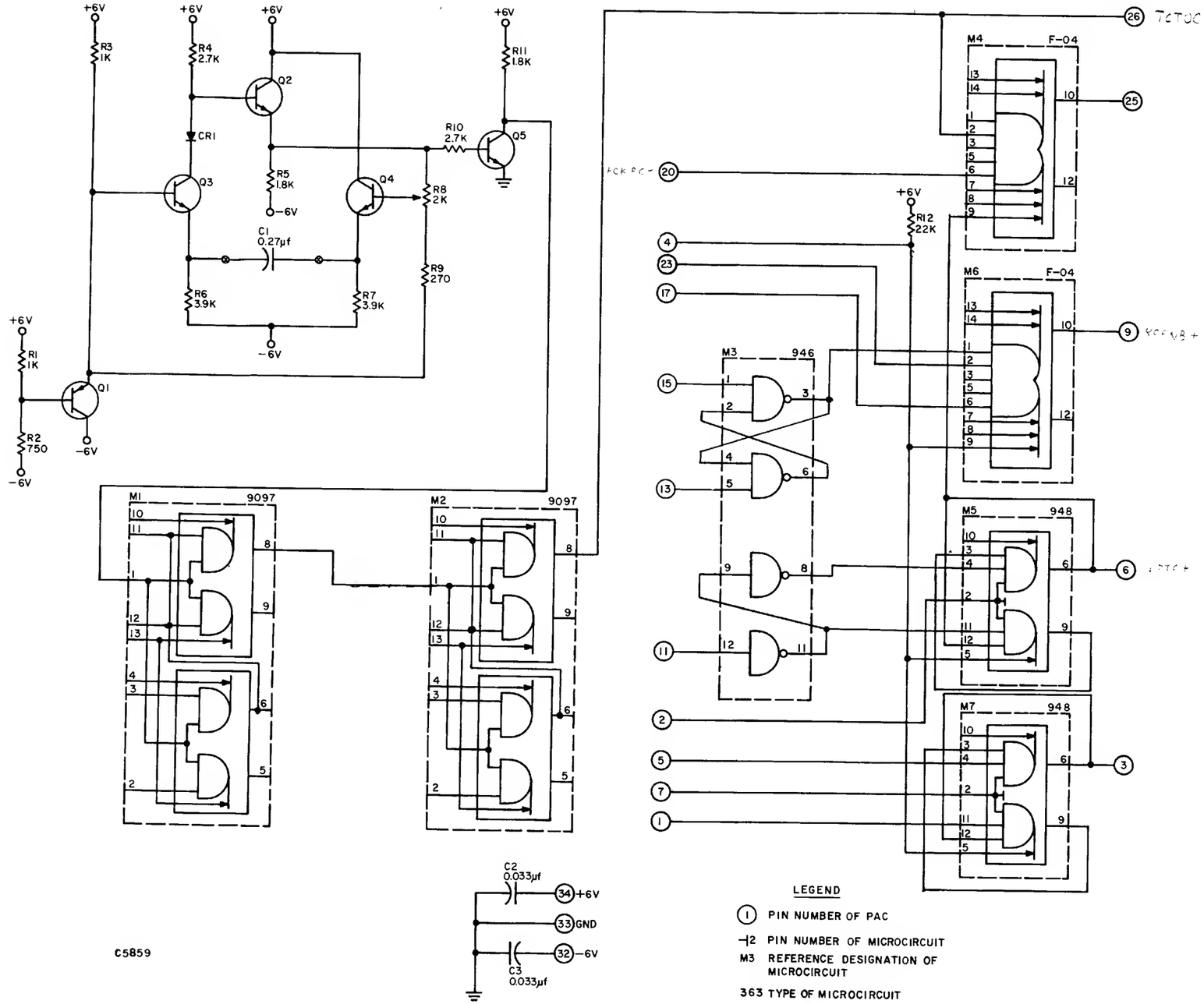

Figure CC-344-1. Real Time Clock PAC, Schematic Diagram

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